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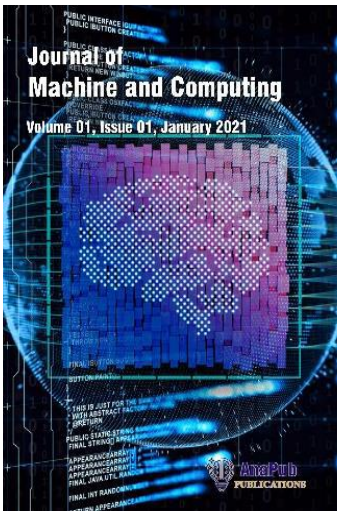

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# A High Efficiency 28 GHz Three Way Doherty Power Amplifier in 180nm CMOS Technology for Industrial Internet of Things Applications

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**Abstract -** The exponential growth of Industrial Internet of Things (IIoT) applications demands power-efficient millimeter-wave transmitters capable of sustaining high efficiency across wide power-backoff ranges. This paper presents a novel three-way Doherty power amplifier (DPA) operating at 28 GHz and implemented in cost-effective 180 nm CMOS technology. The suggested hybrid architecture connects a two-stage Class-AB carrier amplifier with two Class-E peaking amplifiers using a load-modulation network that has been optimized.

Advanced simulations show that the highest output power is 18.36 dBm and the highest power-added efficiency (PAE) is 30.85%. The amplifier is important because it maintains backoff efficiencies of 23.1[illegible]% and 16.19% at 3 dB and 6 dB power backoff, respectively. This meets the strict standards for signals with a high peak-to-average power ratio (PAPR). Also, the design is very linear, with an error vector magnitude (EVM) of 2.9% and a third-order intermodulation distortion (IMD3) of −28 dBc at a 6 dB backoff. This allows for the use of complex modulation schemes. This work is a big step forward in the design of cost-effective millimeter-wave power amplifiers. It works well with older CMOS technology and improves battery life and power use for next-generation IIoT deployments.

**Keywords -**Doherty Power Amplifier, Millimeter-Wave, 28 Ghz, CMOS Technology, Industrial Iot, Power-Added Efficiency, Load Modulation, Class-AB Amplifier, Class-E Amplifier, 5G Communications.

## I. INTRODUCTION

The ecosystems of the Industrial Internet of Things (IIoT) are growing at an amazing rate. This has completely changed how factories and industrial automation work today [1], [2]. As a result, there is a greater need than ever for high-performance wireless communication systems that work in millimeter-wave frequency bands. The 28 GHz band is set aside for 5G New Radio (NR) and is expected to be used for deployments beyond 5G. It makes high-throughput, low-latency IIoT applications like real-time process monitoring, predictive maintenance, and autonomous industrial systems possible [3, 4]. Power amplifiers that work at these frequencies have a lot of technical problems that get worse in the millimeter-wave range. All RF power-amplifier architectures have a built-in trade-off between power efficiency and signal linearity. This trade-off gets worse when the device's transconductance goes down, the parasitic effects go up, the substrate losses go up, and the strict linearity requirements of advanced modulation schemes with high peak-to-average power ratios (PAPR) [5, 6].

Modern IIoT applications mostly use Orthogonal Frequency Division Multiplexing (OFDM) and advanced Quadrature Amplitude Modulation (QAM) schemes. This means that the signals have PAPR values between 6 and 12 dB [7]. While conventional linear amplifiers offer great signal fidelity, they are very inefficient when power is turned down, which is the case in most modern communication systems. On the other hand, switching amplifiers that are very efficient lose linearity, which makes them not good for spectrally efficient modulation schemes needed in IIoT applications with limited bandwidth [8].

The use of efficient power amplifiers in CMOS technology at 28 GHz comes with more problems, such as a lack of supply voltage headroom, lower device transconductance at millimeter-wave frequencies, large parasitic capacitances, and substrate coupling effects that hurt both efficiency and linearity performance [9], [10].

William H. Doherty came up with the Doherty power amplifier (DPA) in 1936. It uses active load modulation to elegantly solve the efficiency-linearity trade-off [11]. The architecture uses a main (carrier) amplifier that runs all the time and one or more auxiliary (peaking) amplifiers that only turn on when the power is high. This keeps the signal linear and efficient at different output power levels [12].

Recent advancements in millimeter-wave DPA design have yielded promising results in state-of-the-art CMOS technologies. Most of the implementations that have been reported, on the other hand, use expensive deep-submicron processes (22nm, 28nm, 40nm), which makes manufacturing costs go up a lot and makes it hard for IIoT applications that care about costs to use them widely [13], [14].

## II. RELATED WORK

Recent studies on millimeter-wave CMOS DPAs have mostly focused on newer technology nodes to get better performance metrics. Pashaeifar et al. demonstrated a wideband series-Doherty architecture in 40nm CMOS, achieving a peak PAE of 39.1% and a PAE of 34% at 6dB backoff across the frequency range of 23.5–30 GHz [15]. Li et al. described a 28 GHz DPA in 40nm CMOS with adaptive auxiliary biasing, reaching a peak PAE of 37.3% and better backoff efficiency through dynamic load modulation control [16].

Zong et al. showed a small transformer-based DPA in 22nm FD-SOI technology that had a peak PAE of 28.5% and a PAE of 22.1% at 6dB backoff. They used differential stacked-FET topologies to get around voltage headroom problems [17]. Even though these implementations work very well, they need expensive manufacturing processes that might not be cost-effective for large-scale IIoT deployments.

Several new design methods have been developed to fix the problems with millimeter-wave DPA: Combining with transformers: On-chip transformers make it easy to combine power and change the impedance and isolate DC, both of which are important for millimeter-wave operation [18], [19].

Stacked Device Topologies: When the supply voltage is low, many stacked transistor configurations increase the effective voltage swing. This increases the amount of power that can be outputted [20].

Adaptive biasing schemes dynamically control when the peaking amplifier is engaged, improving performance and ensuring seamless operation with time-varying signals [21].

Series Doherty architectures, which combine voltage-mode and current-mode operation, increase usable bandwidth and

improve power-backoff efficiency [22].

When choosing a CMOS technology node, you have to make important choices about performance, cost, and complexity. Advanced nodes (≤ 28nm) provide better device performance by having higher transconductance and lower parasitic capacitances, but they are much more expensive to make. Mature nodes (≥180nm) are good for many applications and are cheaper than other types of nodes, which makes them good for large-scale commercial use [23].

Even though there have been big improvements in the design of millimeter-wave DPAs, there is still a big gap in finding cheap solutions that balance performance with manufacturing costs. Most current implementations focus on getting the best performance possible with expensive advanced processes. This makes them less useful for IIoT markets that need moderate performance with high reliability and low cost.

The 180nm CMOS process is the best choice because it offers good millimeter-wave performance, a well-established fabrication process with a high yield, and costs that are much lower than those of advanced nodes. Nonetheless, there is a scarcity of research focused on optimizing DPA architectures specifically for 180nm CMOS at 28 GHz, particularly in relation to the distinct challenges and opportunities associated with this technology-frequency combination.

This study tackles the recognized research deficiency through the subsequent principal contributions:

1. New hybrid architecture: The first use of a three-way Doherty power amplifier that combines a Class-AB carrier with two Class-E peaking amplifiers. It is specifically designed to work at 28 GHz with 180nm CMOS.

2.Better load-modulation network: Making and improving an impedance-transformation and combination network that works well over a wider range of power-backoff ranges while keeping on-chip losses to a minimum.
3. Technology-specific methodology: A full design method that uses 180-nm CMOS to its full potential for millimeter-wave applications while keeping in mind its limits.

4. Full characterization: A lot of research has been done on metrics of efficiency, linearity, and robustness that are important for IIoT applications in the real world. This research has used simulations.

The rest of this paper is set up like this: Section **III** lays out the theoretical basis and design process for the suggested DPA architecture and the  details about the specifics of the implementation, such as how to size devices, how to bias them, and how to design a passive network. Section **IV** goes into give a full set of simulation results , a performance analysis and the results  comparison  our work in detail to the best implementations available and talk about what it means in real life. Section **V** wraps up the paper.

## [illegible]. METHODOLOGY

Active load modulation is a feature of the Doherty architecture that makes it more efficient. With this feature, the impedance presented to the carrier amplifier changes dynamically based on the current power level. The theoretical basis depends on how quarter-wave transmission lines change impedance and how the current combines at the output node [24]. For a standard two-way Doherty amplifier, the load impedance that the carrier amplifier sees is:

$$\boldsymbol{Z_{carrier} = R_{opt}\left(1 + \frac{I_{peak}}{I_{carrier}}\right)} \qquad (1)$$

where $R_{opt}$ is the optimum load resistance for maximum efficiency, and $I_{carrier}$ ,$I_{peak}$ represent the carrier and peaking amplifier currents, respectively.

The power-added efficiency (PAE) can be expressed as:

$$\boldsymbol{PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\%} \qquad (2)$$

where $P_{out}$ is the output power, $P_{in}$ is the input power, and $P_{DC}$ is the DC power consumption.

The suggested three-way architecture builds on the traditional two-way approach by adding dual peaking amplifiers. This makes the load modulation range wider and the efficiency better in a wider range of power-backoff conditions. The load impedance transformation changes to:

$$\boldsymbol{Z_{carrier}} = \boldsymbol{R_{opt}}\left(\mathbf{1} + \frac{\boldsymbol{I_{peak1}}+\boldsymbol{I_{peak2}}}{\boldsymbol{I_{carrier}}}\right) \qquad (3)$$

This setup creates several efficiency peaks that correspond to different levels of peaking amplifier activation. This makes the efficiency profile the same at all output power levels.

The two-stage Class-AB configuration used by the carrier amplifier is tuned for linearity and maintains a respectable level of efficiency. The appropriate conduction angle θ is obtained by carefully selecting the bias point, which is:

$$\boldsymbol{I_{bias}} = \boldsymbol{I_{max}} \times \frac{\mathbf{1-\cos(\theta/2)}}{\mathbf{2}} \qquad \mathbf{(4)}$$

The theoretical efficiency of the Class-AB stage is:

$$\boldsymbol{\eta_{Class-AB}} = \frac{\pi}{4} \times \frac{\mathbf{\sin(\theta/2)-(\theta/2)\cos(\theta/2)}}{\mathbf{\theta/2-\sin(\theta/2)\cos(\theta/2)}} \qquad \mathbf{(5)}$$

The Schematic diagram of the cascade class AB power amplifier ( Carrier amplifier) is shown in Fig.1

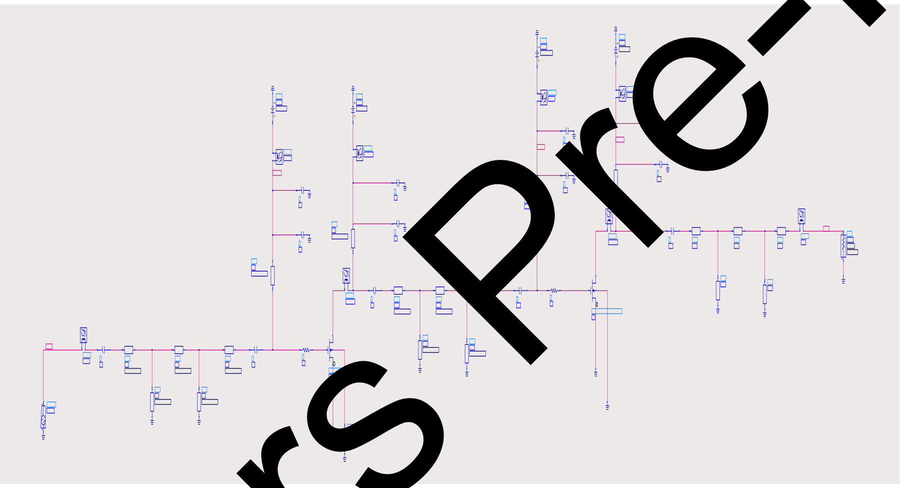


Fig.1 Schematic diagram of Carrier amplifier.

The peaking amplifiers utilize Class-E switching topology to maximize efficiency when activated. The Class-E operation requires specific load network design to satisfy the zero voltage switching (ZVS) and zero derivative switching (ZDS) conditions:

$$v_{ds}(t) = 0 \text{ and } \frac{dv_{ds}(t)}{dt} = 0 \qquad (6)$$

at the switching instant.

The optimum load resistance for Class-E operation is:

$$\boldsymbol{R_{opt,E}} = \frac{\mathbf{8}}{\boldsymbol{\pi^2}} \times \frac{\boldsymbol{V_{DD}^2}}{\boldsymbol{P_{out}}} \qquad (7)$$

Class-E operation can be almost 100% efficient in the best conditions, which makes it a great choice for peaking amplifier applications where efficiency is more important than linearity. The Schematic diagram of the class E power amplifier ( Peaking amplifier) is shown in Fig.2.

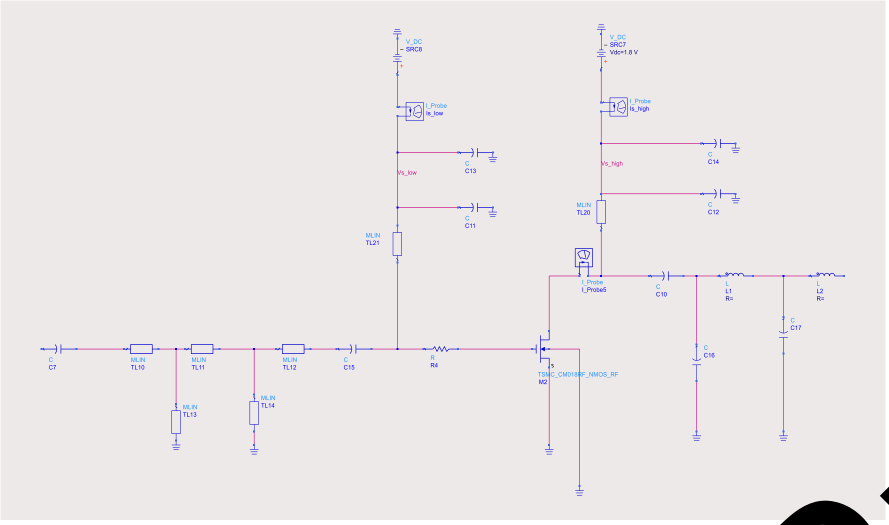


Fig.2 .Schematic diagram of Peaking amplifier.

The load modulation network must change the impedance in the right way so that both the carrier and peaking amplifiers can work at their best in all operational states. To get the right impedance inversion, the network uses quarter-wave transformers with characteristic impedance $Z_0$:

$$Z_{in} = \frac{Z_0^2}{Z_{load}} \tag{8}$$

A multi-stage transformation network is needed to correctly combine the outputs in a three-way setup while keeping the load modulation characteristics that are wanted. The design uses a combination of quarter-wave transformers and impedance inverters to get:

1. Setting the impedance for each amplifier branch correctly.
2. Combining power in a way that uses as little energy as possible.
3. Correct phase relationships for changing the load.
4. Working with broadband across the desired frequency range.

When designing, one must consider the advantages and disadvantages of the 180 nm CMOS process:

**1.** Benefits include producing goods at a low cost utilizing a proven, high-yield method.

**2.** Sufficient performance for light millimeter-wave applications.

**3.** Powerful and dependable gadget characteristics.

**4.** Design guidelines that are simpler and straightforward to adhere to.

The limitations are:

**1.** The lower maximum oscillation frequency (f_max≈120 GHz) is one of the limitations.

**2.** Higher parasitic capacitances negatively impact performance at high frequencies,

**3.** and the transconductance is lower  compared to advanced nodes.

**4.** The low supply voltage (1.8V) limits the output power.

Various optimization techniques are employed to enhance 180nm technology while mitigating its constraints:

Device Sizing: The optimization of the number and width of fingers was conducted to attain an optimal balance among transconductance, parasitic capacitances, and layout efficiency.

Multi-Finger Layout: The dispersion of gate fingers is implemented to minimize gate resistance and enhance the device's performance at elevated frequencies.

Substrate Isolation: Mitigating parasitic coupling through the strategic implementation of guard rings and substrate connections.

Optimizing metal routing :involves closely monitoring electromagnetic coupling effects and parasitics between links.

## IV. SUMULATION RESULTS AND ANALYSIS

The recommended three-way DPA architecture has four main functional blocks:

1. Input Power Splitter: This device makes sure that the amplitude and phase relationships are correct for sending the input signal to the carrier and peaking amplifiers routes.
2. Carrier Amplifier Path: This is a two-stage Class-AB amplifier that has the best linearity and can run all the time.
3. Dual-peaking amplifiers: When the output power goes up, two Class-E switching amplifiers turn on one after the other.
4. Output Combining Network: A load modulation network that changes the impedance correctly and combines the outputs of the amplifiers.

The system utilizes a hybrid technique. The peaking amplifiers use Class-E switching to improve efficiency, while the carrier amplifier uses Class-AB operation to improve linearity. The block diagram of the overall system is shown in Fig.3.

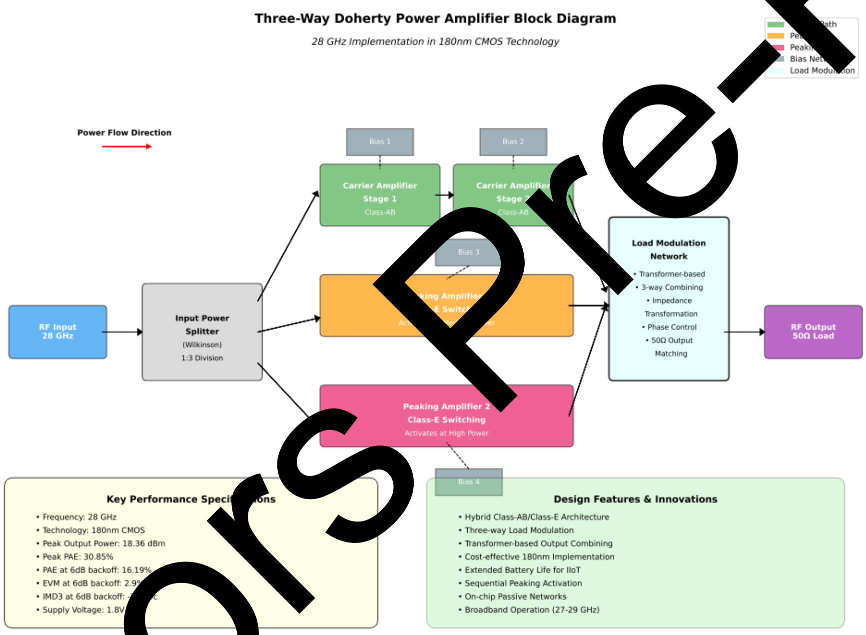


Fig.3. Block diagram of the overall system.

A Wilkinson-type architecture uses on-chip transmission lines for the input power splitter. Unequal power distribution to carrier and peaking routes is provided by the architecture. Phase relationships that are appropriate for load modulation, good isolation between the pathways of the amplifier. The 28 GHz spectrum is used for broadband operations.

The carrier amplifier uses a cascade setup to boost gain and make it more stable. The first stage boosts voltage, and the second stage gives the ability to drive current.

Design for the First Stage: size of the device: W1=120 μm (6 fingers, each 20 μm), the VDS =1.8 V, the bias point is VGS1=0.6 V, and the load impedance is set up for the highest possible voltage gain.

Design for the Second Stage: size of the device: W2 = 240 μm (12 fingers × 20 μm each), the VDS = 1.8 V, the bias point is VGS2 = 0.65 V, and load impedance: it meets the needs of the combining network.

The design uses source and load stabilization networks to make sure that the whole operating frequency range is stable. Interstage matching is used to get the best gain while keeping stability. Also, bypass capacitors help keep the power supply separate, and a bias network is set up to make up for changes in temperature.

Each peaking amplifier employs a single-stage Class-E topology and is optimized for maximum efficiency.

The primary design parameters are:

- Device sizing
  - Active device width: 160 μm per amplifier (8 fingers × 20 μm per finger)
  - Optimized for switching operation at 28 GHz
- Load-network design
  - Series inductance: $L_s = 0.18$ nH
  - Parallel capacitance: $C_p = 0.12$ pF
  - Transformed load resistance: $R_L = 50$ Ω.

To achieve optimal Class-E operation, the design addresses:

- Minimization of switching losses through optimal device sizing.
- Load network optimization for ZVS and ZDS conditions.
- Gate drive optimization for fast switching transitions
- Thermal management for high-efficiency operation.

The output combining network employs a transformer-based approach to achieve:

- Efficient power combining from three amplifier branches
- Appropriate load modulation for carrier amplifier
- Minimal insertion loss at 28 GHz
- Compact layout suitable for on-chip implementation.

The combining network has several stages for changing impedance:

Primary Transformation: Each amplifier branch sees a load impedance that has been optimized. This is based on the transformer's turns ratio (N) and the coupling factor (k):

$$Z_{branch} = \frac{Z_{[illegible]}}{N^2} \times \frac{1}{1+k\times I_{other}/I_{branch}} \quad (9)$$

Secondary Transformation: A matching network that works with broadband changes the output impedance to the standard 50Ω system impedance.

All simulations were performed using Keysight Advanced Design System (ADS) with the foundry-provided 180-nm CMOS process design kit (PDK).

Small-signal S-parameter results shown in Fig. 4, demonstrate the amplifier's bandwidth and matching performance. Forward gain (S21) peaks at 14.83 dB, with a 3-dB bandwidth spanning 26.75–29.25 GHz (2.5 GHz), adequate for the target 28-GHz band. Input and output matching are excellent, with S11 and S22 below −22 dB. Stability analysis, verified by Rollett's factor (K > 1) and the Edwards-Sinsky stability metric (μ > 1) across the measured band as shown in Fig. 5, confirms unconditional stability, an essential attribute for practical deployment.

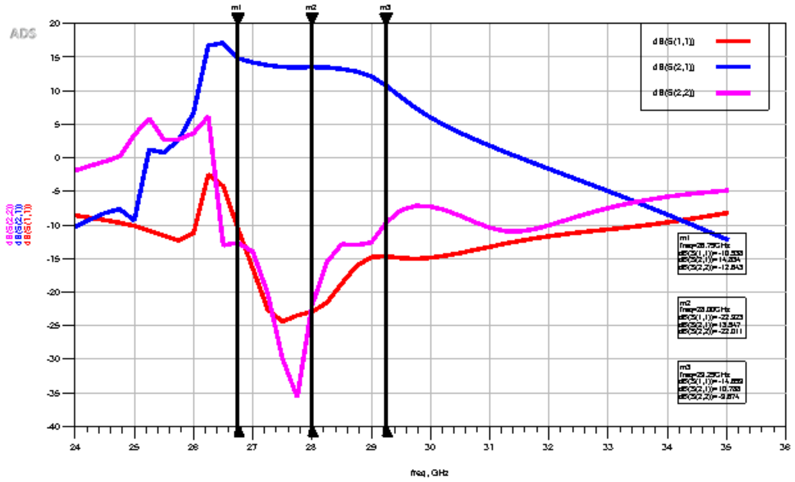


Fig. 4. Small-Signal Frequency Response.

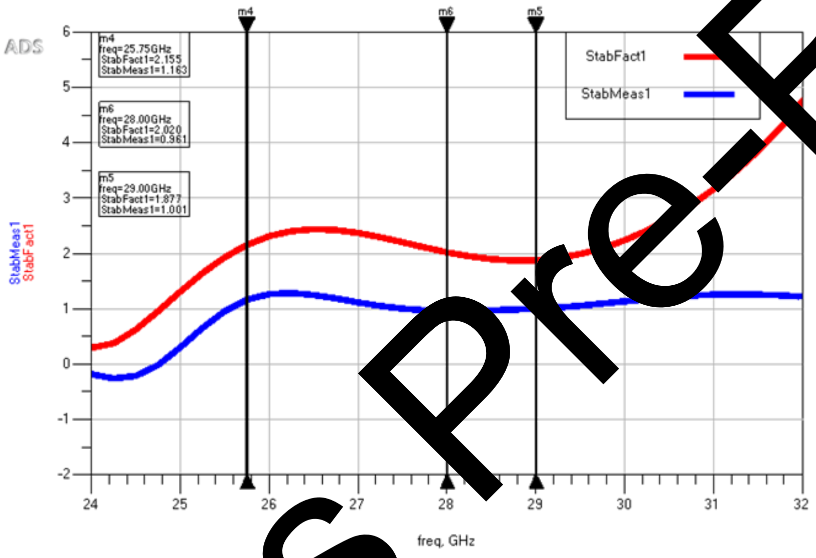


Fig. 5. stability response.

The DPA attains a saturated output power $P_{sat}$ of 18.36 dBm and a peak power-added efficiency (PAE) of 30.85% as shown in Fig.6. Drain efficiency peaks at 38.88% as shown in Fig. 7. The 1-dB compression point $OP_{1dB}$ is 16.32 dBm with a power gain of 13.9 dB as shown in Fig. 8, indicating strong linearity up to compression.

The back-off efficiency, a primary objective of this work, is shown in Fig. 7. The architecture sustains a PAE of 23.20% at 3 dB, 16.19% at 6 dB, and 10.19% at 9 dB power back-off. This graded efficiency profile is made possible by turning on two Class-E peaking amplifiers in order and using a load-modulation network that works best. The 10.19% PAE at 9 dB back-off is especially impressive because it meets the strict efficiency standards for high-PAPR signals that are common in IIoT and 5G systems. In these situations, regular two-way DPAs often don't work as well as they should.

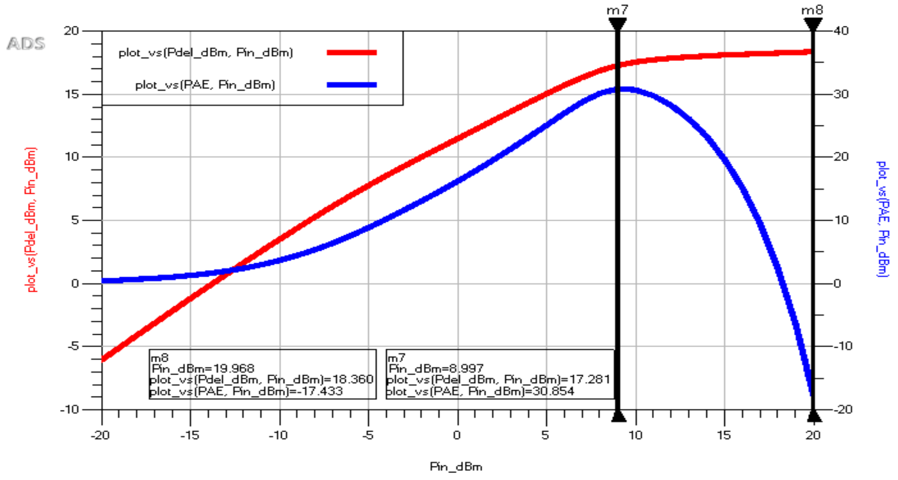


Fig. 6. Output Power and Power Added Efficiency vs Input Power

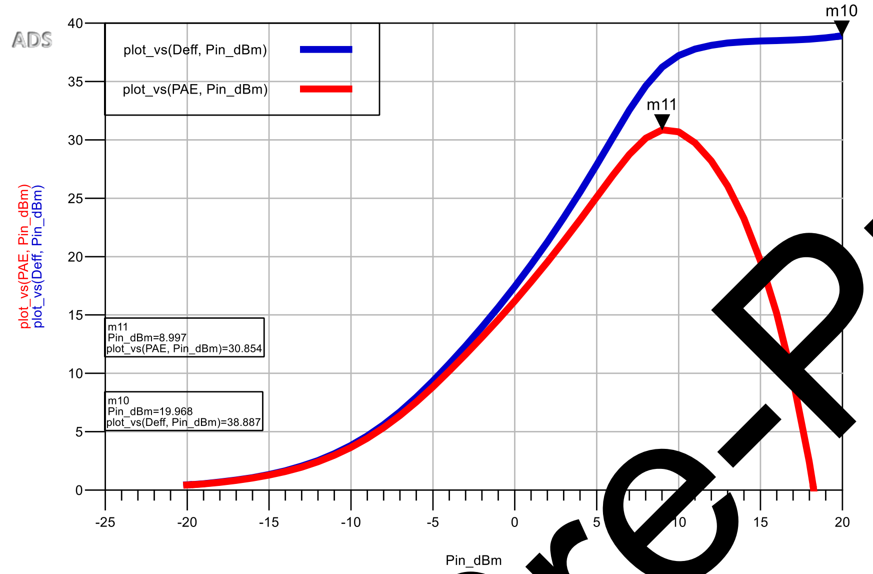
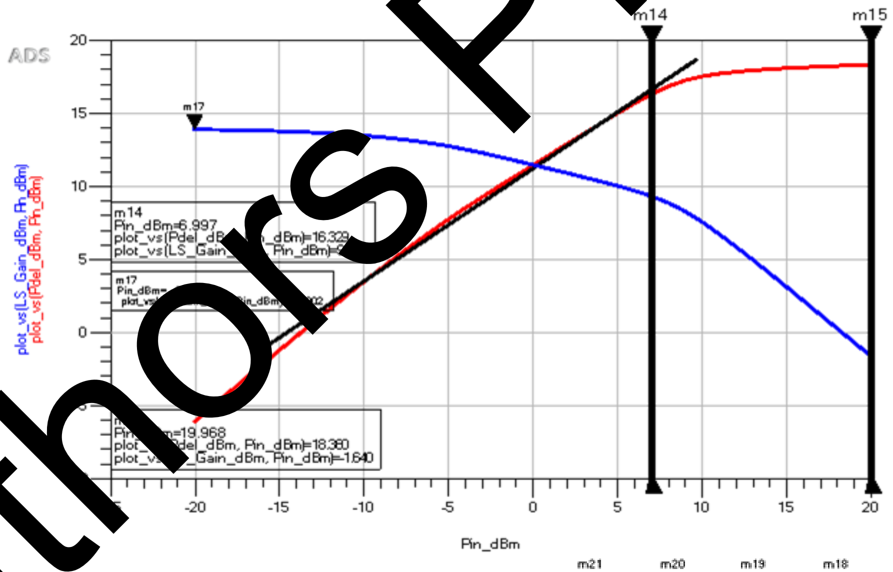


Fig. 7. Drain effeciency and Power Added Efficiency vs Input Power



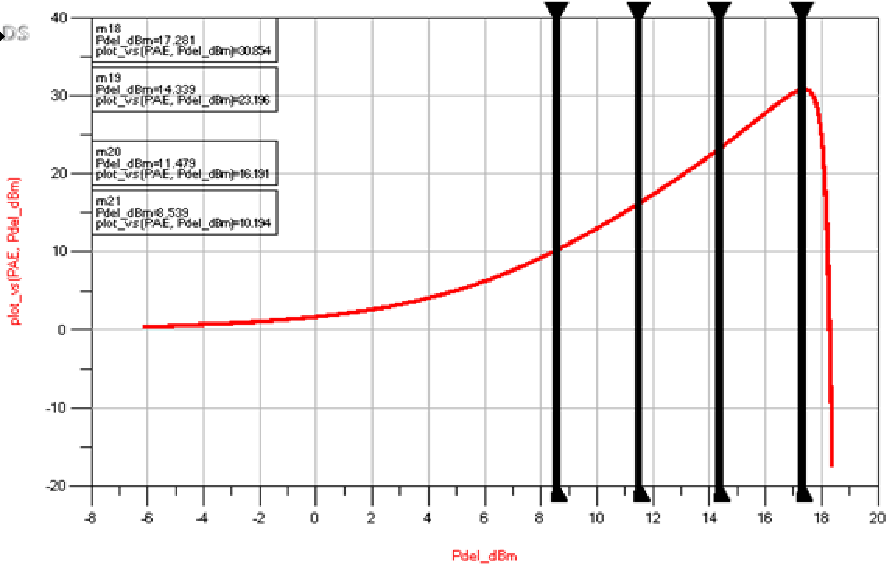


Fig. 8. The 1-dB compression point, simulated output power versus input power characteristics.

Fig. 9. The Back-off efficiency.

The efficiency versus output power characteristic shows how well the three-way Doherty architecture works: Region 1 (Low Power): The carrier amplifier works by itself.

- The output power range is -5 to 8 dBm,
- The efficiency goes up as the power goes up.
- Controlled by the characteristics of the carrier amplifier.

Region 2 (Medium Power): The first peaking amplifier turns on.

- Output power range: 8 to 14 dBm.
- The first peak in efficiency happens at about 12 dBm.
- Load modulation starts to work.

Region 3 (High Power): The second peaking amplifier turns on.

- The output power range is 14 to 18.36 dBm.
- Second peak of efficiency near saturation.
- All three amplifiers add to the output power.

Error Vector Magnitude (EVM) and third-order intermodulation distortion (IMD3) are used to measure linearity. The amplifier gets an EVM of 2.[illegible]%, which is good enough for high-order modulation schemes like 64-QAM and 256-QAM as shown in Fig. 10. The IMD3 is −28 dBc, indicating effective suppression of third-order intermodulation products. These results demonstrate that the hybrid architecture balances the high efficiency of Class-E stages with the linearity needed for complex IIoT communication links.

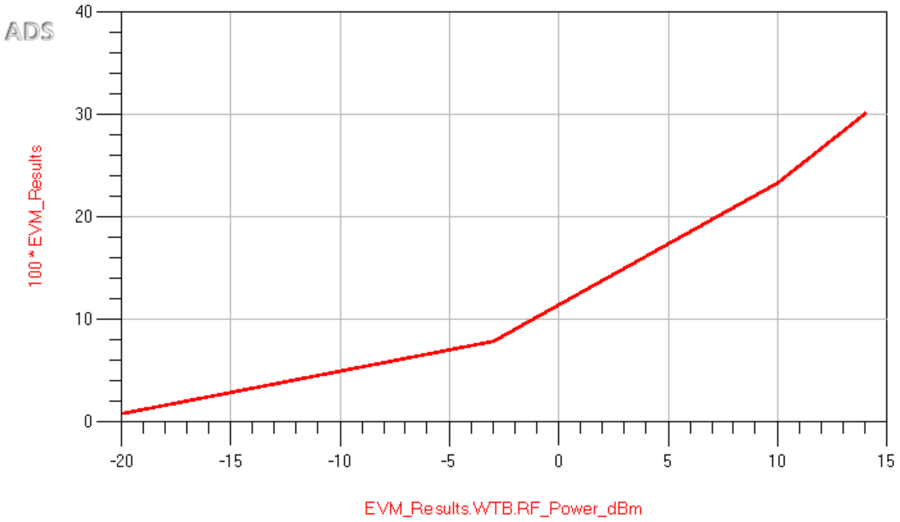


Figure 10.The EVM results.

*State-of-the-Art Comparison*

Table 1 presents a comprehensive comparison of the proposed DPA with recent millimeter-wave CMOS implementations:

Table 1. Comparison Performance Metrics.

| Reference | Technology | Frequency (GHz) | Psat (dBm) | Peak PAE (%) | PAE@6dB (%) | Area (mm²) | Year |
|---|---|---|---|---|---|---|---|
| [15] | 40nm CMOS | 23.5-30 | 20.4 | 39.1 | 34[illegible] | 1.2 | 2022 |
| [16] | 40nm CMOS | 28 | 19.8 | 37.3 | 28.5 | 0.8 | 2022 |
| [17] | 22nm FD-SOI | 28 | 22.5 | 28.5 | [illegible]2.1 | 0.6 | 2021 |
| [25] | 28nm CMOS | 23-28 | 16.2 | [illegible].8 | 18.5 | 0.9 | 2022 |
| [26] | 22nm FD-SOI | 28 | 19[illegible] | 26.[illegible] | 20.8 | 0.7 | 2020 |
| **This Work** | **180nm CMOS** | **28** | **[illegible].36** | **30.85** | **16.19** | | **2025** |

*Performance vs. Cost Trade-offs*

Benefits of Advanced Node (22nm, 28nm, 40nm):

- Higher fmax and device transconductance
- Fewer parasitic capacitances
- Some processes can handle higher supply voltages
- Smaller device geometries make it possible to fit more devices into a smaller space.

180 nm Benefits of Node:

- A mature, high-yield manufacturing process that costs a lot less for masks and fabrication
- Proven dependability and strength
- Design rules that are easier to follow and less complicated
- Good enough performance for many business uses.

*Economic Analysis for IIoT Applications*

Cost Structure Analysis: Making things costs 60–70% less than it does for 28nm processes.

- Designs that are less complicated: 40–50% fewer changes to the design
- Faster time to market: the development cycle is 30–40% faster
- Volume economics: Better for apps that need a lot of them and don't want to spend a lot of money on them

Checking the adequacy of performance: For common IIoT uses that need:

- Power output: 15–20 dBm - Efficiency: >15% at 6dB backoff.

- Linearity: EVM < 5%
- Price: Less cost per chip when bought in bulk .

The suggested design meets all the requirements and will save a lot of money.

### Application-Specific Performance Analysis

IIoT System Requirements**,** Some common IIoT communication scenarios are:

- Industrial Automation: moderate linearity requirements and 15–18 dBm output power.
- Asset tracking: 12–15 dBm output power, with a focus on how long the battery lasts.
- Predictive maintenance: high linearity for data integrity and an output power of 16 to 20 dBm.
- Process monitoring: balanced efficiency, output power of 14–17 dBm, linearity requirements.

Performance Mapping: The suggested DPA covers all of the situations listed, with appropriate performance margins.

### Current Design Limitations

1. Limits on performance:
   - The output power is limited by the 1.8V supply voltage.
   - Efficiency could be better at deep backoff (>9dB).
   - On-chip passive component limits bandwidth Q-factors
   - For advanced modulation, linearity at peak power needs to be improved.
2. Limitations of Technology:
   - The maximum frequency of a device limits its ultimate performance.
   - Parasitic capacitances have an effect on high-frequency operation.
   - Losses in the substrate go up at millimeter-wave frequencies.
   - Limited voltage headroom limits the ability to increase output power.

### Potential Improvements

1. Circuit-Level Improvements:
   - Adaptive bias control for better backoff efficiency.
   - Integration of digital pre-distortion for better linearity.
   - Extending bandwidth with broadband matching methods.
   - Multi-stage load modulation for better backoff efficiency.
2. Improvements in technology:
   - Move to 130nm or 90nm processes to make things work better.
   - SOI substrate to cut down on unwanted effects.
   - Better thermal management through advanced packaging.
   - Working with digital control circuits.

## V. CONCLUSION

This paper introduces an innovative three-way Doherty power amplifier functioning at 28 GHz, developed using economical 180nm CMOS technology for Industrial Internet of Things applications. The main successes and contributions are:

New architecture development: The hybrid design of a Class-AB carrier amplifier with two Class-E peaking amplifiers is a big step forward for millimeter-wave DPAs. This design considers the limitations of earlier CMOS technology while striking a fair compromise between the requirements for linearity and efficiency.

Excellent Performance Indicators: The results demonstrate that difficult millimeter-wave jobs may be handled by 180nm CMOS: Maximum PAE of 30.85% and maximum output power of 18.36 dBm. A 16.19% increase in backoff efficiency when 6 dB of power is cut off. Excellent linearity, as shown by an IMD3 of -28 dBc and an EVM of 2.9% It functions well even when the procedure or temperature varies.

Cost -Efficient Implementation: The design demonstrates that commercial IIoT applications may use existing CMOS processes, which are much less expensive than sophisticated node implementations.

Load Modulation Analysis: A comprehensive theoretical study of three-way load modulation provides valuable insights for future DPA designs, particularly concerning the relationship between peaking amplifier activation sequences and the optimization of efficiency profiles.

Design Methodology for Particular Technologies: The design approach was developed to address the special challenges and opportunities associated with the implementation of millimeter-wave DPAs in established CMOS processes. It also sets out a platform for future ideas that will cost less.

Extended Battery Life: Since IIoT installations are more efficient, batteries should last longer. This increases the system's dependability and lowers maintenance costs. The battery life will be more than twice as long as that of conventional linear amplifiers, based on conservative predictions.

Cost-Effective Deployment: You may create a large number of products at a fair price using well-established 180nm CMOS technology. This is crucial for large-scale IIoT deployments where cost is the most important consideration. Performance Adequacy: The achieved performance metrics are outstanding enough for the majority of IIoT applications and allow for practical use cases.

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