Experimental Investigation of Modified Level Shift PWM With Capacitor Voltage Balancing on Single Phase Modular Multilevel Converter

[1]Balamurugan S, [2]Bhavani M, [3]Sudha R and [4]Padmanaban K
[1]Department of EEE, Government College of Technology, Coimbatore, Tamil Nadu, India.
[2]Department of EEE, Government College of Srirangam, Trichy, India.
[3]Department of EEE, Thanthai Periyar Government Institute of Technology, Vellore, Tamil Nadu, India.
[4]Department of EEE, Alagappa Chettiar Government College of Engineering and Technology, Karaikudi, India.
[1]sbalaaccet@gmail.com, [2]mbhavanieee@gmail.com, [3]gosudha@gmail.com, [4]padupoi@gmail.com

Correspondence should be addressed to Balamurugan S: sbalaaccet@gmail.com

Article Info
Journal of Machine and Computing (http://anapub.co.ke/journals/jmc/jmc.html)
Doi: https://doi.org/10.53759/7669/jmc202404072
Received 29 October 2023; Revised from 16 March 2024; Accepted 24 June 2024
Available online 05 July 2024.
©2024 The Authors. Published by AnaPub Publications.
This is an open access article under the CC BY-NC-ND license. (http://creativecommons.org/licenses/by-nc-nd/4.0/)

Abstract – Modular Multilevel Converters (MMCs) are a prominent voltage source converter topology that is rapidly gaining popularity in medium/high power/voltage applications, including high-voltage DC transmission systems and electric vehicle systems. However, MMC has the critical issue of unbalanced submodule capacitor voltages and circulating current. The MMC distributes DC-link energy evenly among its submodule capacitors, rather than storing it in a large capacitor like conventional voltage source converters. In MMC, the submodule floating capacitors interface the DC input voltage and AC output voltage. Therefore, capacitor voltages must be balanced. The existing capacitor voltage control struggles to handle many gate pulses at medium and high voltages. An effective control scheme is needed to solve the issues mentioned earlier. This paper presents a performance analysis of a 1-Φ MMC using a modified level shift PWM technique based on Universal Control Modulation Scheme (UCMS) and a sorting-based capacitor voltage balancing algorithm. MATLAB/Simulink software implements the proposed control method for a 1-Φ, seven-level MMC. The outcomes of the simulation demonstration reveal that phase disposition PWM offers less harmonic distortion of output phase voltage than the other level shift PWM techniques, such as phase disposition PWM and alternate phase disposition PWM. The simulation results also demonstrate the effective use of the sorting-based capacitor balancing algorithm to regulate the voltages of the submodule capacitors. Finally, the real-time GUI tool validates the simulation results using an experimental prototype of 1-Φ MMC with the dSPACE MicroLabBox 1202.

Keywords – Multilevel Converters, Multi Carrier PWM Method, Sorting Based Capacitor Voltage Balancing, Real Time Interface.

I. INTRODUCTION

At present, the MMC is a fast-emerging technology. Moreover, it is receiving wide acceptance from industry and academia due to its distinct features. The MMC offers numerous benefits compared to other multilevel converter designs, such as its modular and scalable structure to accommodate different voltage levels, the lack of need for isolated DC sources, exceptional efficiency, and excellent harmonic performance. The first commercial implementation of MMC technology in high voltage DC transmission was introduced in 2010.

Then researchers began to recognise the MMC's potential and benefits. It is not only confined to high-voltage DC applications; it is also being proposed for integrating photovoltaic or battery systems into grid-connected applications, medium power/voltage motor drives, flexible AC transmission systems and other applications [1]. The MMC, on the other hand, faces important challenges, such as balancing of submodule capacitor voltages, managing circulating currents, and controlling the capacitor voltage ripples Numerous research studies have focused on MMC control processes to regulate various system efficiency parameters. However, because the MMC structure is new to the market, there is still limited knowledge between engineering development and academic interests. Therefore, it is possible to have an excellent opportunity to improve control technologies and strategies in MMC [2].

The **Fig 1** illustrate structure of a MMC with 1-Φ and a submodule (SM). A MMC' phase leg consists of many identical SMs. To synthesize the required output AC voltage from MMC, the power semiconductor switches in the

submodules are triggered with proper gating pulses. The modulating pulse width techniques are used to apply these pulses for switching the SMs [3]. Furthermore, it regulates the number of SMs that should be activated in the lower and upper arms. Every MMC application needs control mechanisms for balancing the voltage of the submodule capacitor, limiting circulating currents, controlling output current, and reducing submodule capacitor voltage ripples. The purpose of using PWM techniques in a MMC is to minimise the distortion of output voltage harmonics and increase the magnitude of the output voltage at a specific switching frequency. Multi-carrier PWM method is classified into phase-shifted (PS-PWM) and level-shifted (LS-PWM) carrier modulations based on the arrangement of the carriers [4-7]. In general, the carrier based PWMs are uncomplicated and can be readily implemented on digital control platforms. Nevertheless, the alteration in the quantity of submodules impacts the arrangement of carriers in the modulation scheme. Therefore, it is imperative to revamp the carrier PWM modulator to align with the converter's configuration [8-11].

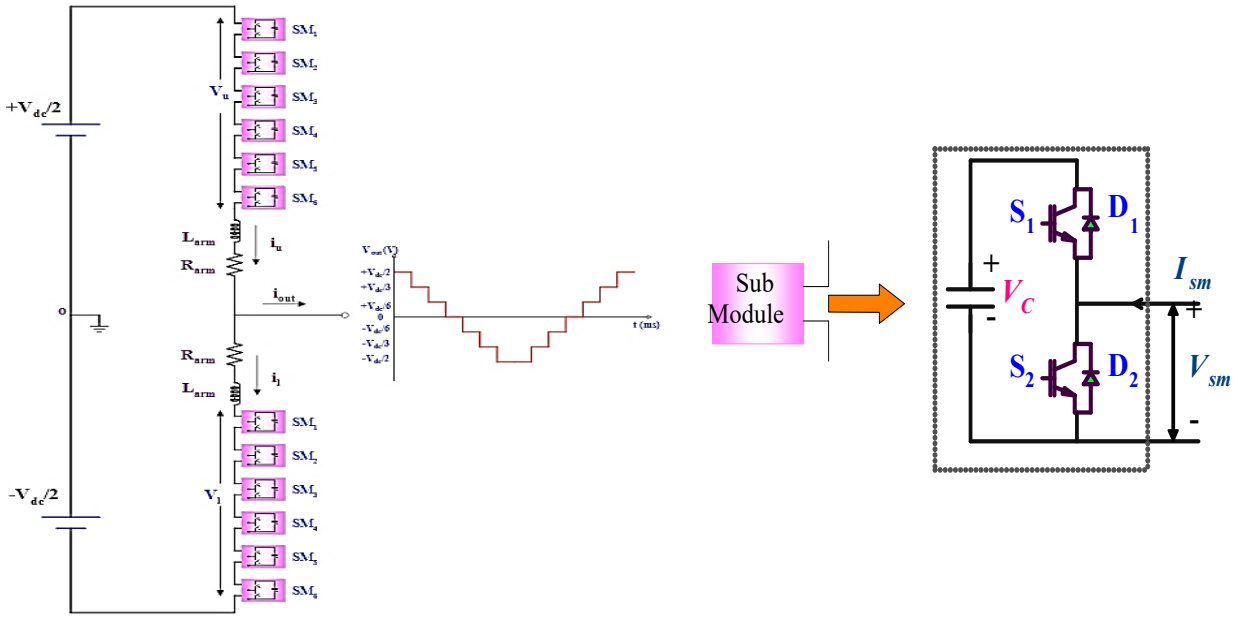


Fig 1. (A). Structure Of 1-Φ Seven Level MMC (B). Structure Of Half-Bridge Submodule.

An important issue with MMC involves the existence of uneven voltages across the submodule capacitors. In MMC, DC link's energy is distributed evenly across the submodule's capacitors, rather than being stored in a single large capacitor like conventional voltage source converters. In the MMC system, the floating capacitors act as a link with the input (DC voltage) and the output (AC voltage). Consequently, it is imperative to guarantee that the capacitors' voltages are equal. To ensure proper functioning, the SM capacitor's voltage must be kept at V_{dc}/m, where m denotes the submodule's number in an arm [12-15]. The voltage balancing of the floating capacitors cannot be ensured by the pulse width modulator, as it does not take into account the voltage of the submodule capacitor various controllers, including leg voltage control, PI, PID, PR, and resonant controllers, are used to maintain a balanced voltage across the capacitor [16]. The existing capacitor voltage control struggles to handle many gate pulses at medium and high voltages.

This work presents the performance analysis of a Universal Control Modulation Scheme (UCMS) based modified level shift PWM (LS-PWM) technique on seven level single –phase MMC. This chapter also describes balancing the SM's capacitor voltage based on the sorting algorithm for MMC.The power distribution among the submodules of the MMC is uneven in the existing LS-PWMs methods. This results in an escalation of harmonic distortion and an imbalance in capacitor voltage. The voltage balancing of the floating capacitors cannot be guaranteed by the pulse width modulator, as it does not take into account the voltage of the submodule capacitor. In order to achieve voltage balance in the capacitor, it is crucial to modify the switching pattern based on the voltage level, arm current, and submodule capacitor voltage. This work implements an efficient modification in LS-PWM using UCMS to address the limitations of modulation methods. The proposed UCMS ensures equal power distribution across all MMC submodules.

Hence the output voltage THD can be reduced. The main contribution of the proposed approach is

- To apply UCMS based modified LS-PWM technique for 1-Φ 7 level MMC and to analyze the performance of harmonic distortions.
- To implement sorting based capacitor voltage balance algorithm for regulating the MMC's submodule voltage.
- The simulation demonstration results indicate that UCMS based phase disposition LS-PWM exhibits lower harmonic distortion in the output phase voltage compared to other LS-PWM techniques, such as phase disposition PWM and alternate phase disposition PWM.

- The simulation outcomes are verified by the real-time GUI tool using an experimental prototype of 1-Φ MMC and the dSPACE MicroLabBox 1202.

The subsequent sections of this paper are structured in the following manner: Section 2 outlines the proposed methodology, Section 3 discusses the simulation analysis, Section 4 details the hardware validation, and Section 5 concludes the research work.

II. PROPOSED METHODOLOGY

This section details the implementation of Universal Control Modulation Scheme (UCMS) based modified LS-PWM schemes: PD, POD and APOD. **Fig 2** illustrates the implementation of the proposed UCMS based LS- PWM in MMC. The power and voltage levels of the MMC increase in proportion to the number of submodules connected in series. The role of these redundant SMs depends on the modulation technique used. This analysis evaluated the total harmonic distortion (THD%) of the output voltage, switching frequency, and modulation scheme. Therefore, suitable multi-carrier-based PWMs are utilised to address different challenges in the MMC. Various multi-carrier PWM strategies can be obtained based on the position, size, and frequency of the carrier signals, as well as the duration of their overlap.

This study examines the performance analysis of a modified LS-PWM technique based on a UCMS applied to a seven-level 1-Φ MMC. This chapter also presents a sorting-based algorithm for balancing the voltage of capacitors in a MMC.The existing level shift PWM methods result in an uneven distribution of power among the submodules of the MMC. This leads to an increase in harmonic distortion and an imbalance in the voltage across the capacitor. This work presents a highly effective modification in the LS-PWM technique by incorporating UCMS to overcome the limitations of existing modulation methods. The proposed UCMS guarantees equitable distribution of power among all MMC submodules. Therefore, it is feasible to decrease the total harmonic distortion (THD%) of the output voltage.

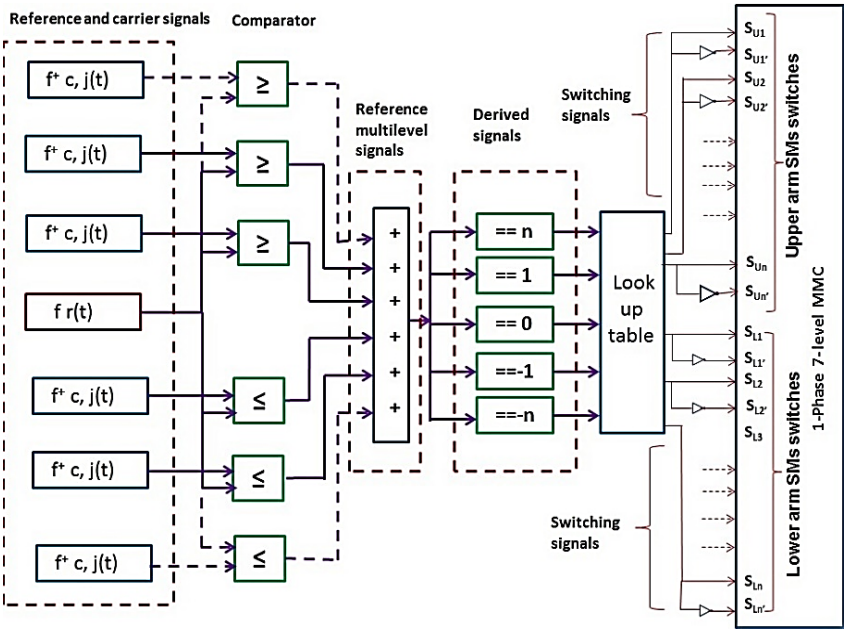


Fig 2. Implementation UCMS Based Level Shift PWM in MMC.

Multi carrier-based PWM techniques are classified based on the position of the carrier signals: level-shift (LS) PWM and phase shift (PS) PWM. The carrier signals in the LS PWM are shifted vertically, whereas those in the PS PWM are shifted horizontally. This LS PWM method employs $n-1$ triangle signals as carriers that are shifted vertically (where n = output voltage's levels) and have the same magnitude $(1/n)$ and frequency (f_c). The gating pulses are generated by comparing the magnitude of the specified carrier signal with the sinusoidal reference signal. In the LS PWM, The equivalent switching frequency (f_{sw}) of the pulses at the output is the same as the carrier frequency (f_c). The classification of LS-PWM according to the arrangements of carriers is given as follows.i. Phase Disposition (PD), ii. Phase Opposition Disposition (POD), iii. Alternate Phase Opposition Disposition (APOD).

In PD PWM method, all the carrier signals (triangular) have the same phase (in-phase) above and below the zero axis. The number of carrier signals required to generate n levels in the output voltage is $n-1$. Six number of carrier signals generate seven levels in the output voltage ($\pm\frac{V_{dc}}{2}$, $\pm\frac{V_{dc}}{3}$, $\pm\frac{V_{dc}}{6}$, 0). The phase shift angle between the carriers for the upper arm and the carriers for the lower arm should be 180º. **Fig 3 (a)** illustrate the pulses generated for each carrier PD PWM. The resultant pulse consists of six levels varying from magnitude zero to six.

In POD PWM method, all carriers above zero level are in-phase to each carriers and while being 180-degree phase shift to the carriers below zero level. For seven-level output, six carriers (C_1, C_2, C_3, C_4, C_5 and C_6) are placed vertically

with carrier frequency f_c. This PWM technique has a sine reference signal with angular frequency 2πf, Where f is the fundamental frequency 50 Hz. **Fig 3 (b)** shows the pulses generated for each carrier in UCMS-PD PWM. The resultant pulse consists of six levels varying from magnitude zero to six.

In APOD PWM method, all carriers have 180-degree phase difference from the adjacent carrier in the below and the above zero axis [23]. For seven-level output, six carriers (C_1,C_2, C_3, C_4,C_5 and C_6) are placed vertically with carrier frequency f_c. This PWM method has a sine wave reference signal with angular frequency$2\pi f$, Where f is the fundamental frequency 50 Hz. **Fig 3(c)** illustrates the summation of individual pulses of APOD PWM. The resultant pulse consists of six levels varying from magnitude zero to six.

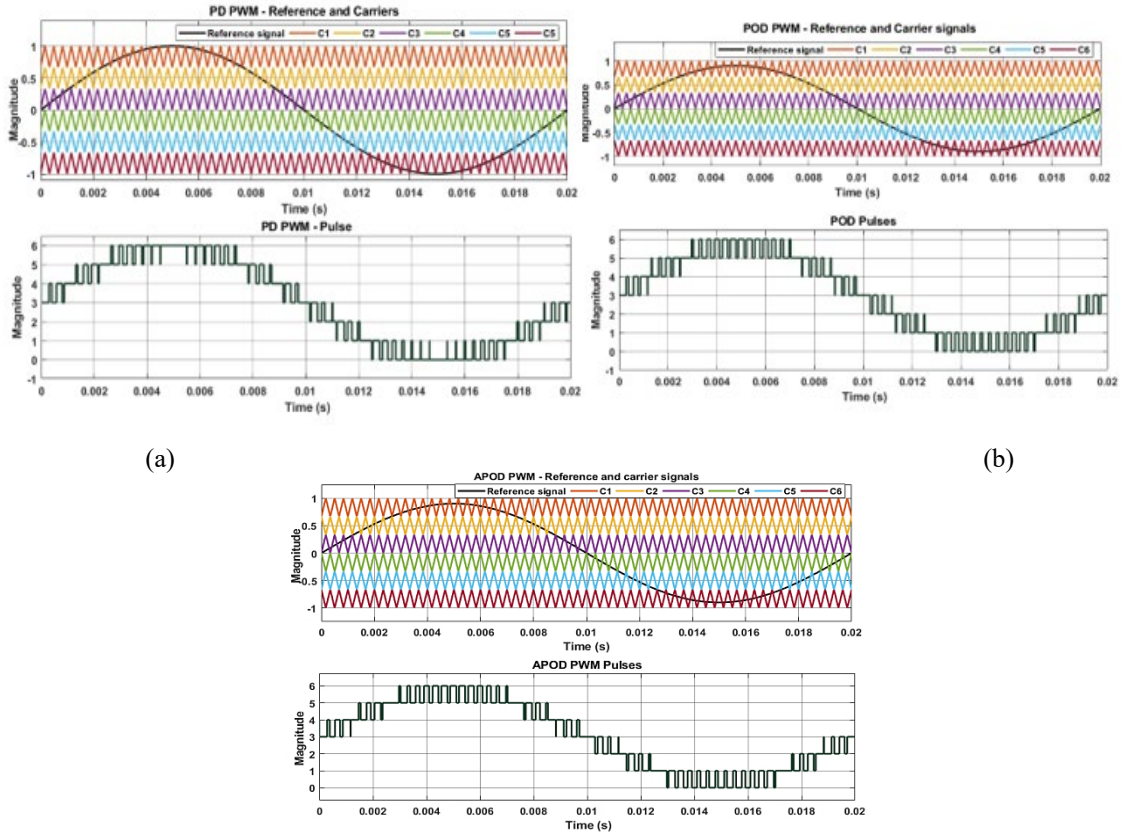


Fig 3. Reference, Carriers and Equivalent Pulse In (a) PD-PWM (b) POD-PWM and (c) APOD -PWM.

III. IMPLEMENTATION OF UCMS BASED MODIFIED LS-PWM IN MMC

Usually, as the voltage and power values of the MMC escalate, there is a corresponding rise in the quantity of interconnected submodules arranged in series. The function of these redundant submodules alters depending on the modulation method employed. This analysis assesses the harmonic content (THD %) of the output voltage, modulation scheme and switching frequency [23-25]. This section describes the implementation of LS-PWM methods: PD, POD and APOD. In the implementation scheme, the reference signals $f_r(t)$ is the sinusoidal signal having amplitude A_r and frequencyω_r. The carrier signal required is $(n-1)$ for the n number of output levels. $f_{c,j}^{+}(t)$ and $f_{c,j}^{-}(t)$,$\{j = 1\ to\ n\}$ represent the carrier signals of below and above the zero reference respectively. It can be computed as,

$$m_f = w_c/w_r \tag{1}$$

$$m_a = A_r/nA_c \tag{2}$$

Where $m_a$and m_f represents the amplitude modulating index and frequency modulating index.

At every instant, the reference signal undergoes comparison with triangle carrier signals. When the magnitude of sinusoidal reference signal exceeds the carrier, it can be represented as "1". Otherwise zero in all carrier signals above zero reference. When the sinusoidal reference signal is greater than the carrier, it can be represented as "0". Otherwise "-1" in all carrier signals below zero reference.

$$f_o^+, (j(t) \ = 1, \ for\ f_r(t) \geq f_c^+, j(t) \\ = 0, \quad \text{otherwise} \tag{3}$$

$$f_o^-, (j(t) \ = 0, \quad for\ f_r(t) \geq f_c^-, j(t) \\ = 0, \quad \text{otherwise} \tag{4}$$

The results of multilevel reference signal is represented as $S_{ML}(t)$ formulated by,

$$S_{ML}(t) = \sum_{j=1}^{n}\{f_o^+, j(t) + f_o^-, j(t)\} \tag{5}$$

$f_{d,j}(t)$ is formulated from $S_{ML}(t)$ using following criteria

$$f_{d,j}\,(t) = 1, \quad if\ s_{ML}(t) = = j \\ = 0, \quad otherwise;\ where,\ j = -n\ to + n \tag{6}$$

Where $f_{d,j}(t)$ denotes the derived pulses. It is formulated from $S_{ML}(t)$ using a lookup table and logic circuits. The lookup table delineates the MMC's switching configurations to attain the required output voltage level, as depicted in **Table 1**.

Table 1. Lookup Table of Switching Pattern For 1-Phase Seven- Level MMC

States	Upper arm SMs						Lower arm SMs						Output levels
	S_{U1}	S_{U2}	S_{U3}	S_{U4}	S_{U5}	S_{U6}	S_{L1}	S_{L2}	S_{L3}	S_{L4}	S_{L5}	S_{L6}	
1	0	0	0	0	0	0	1	1	1	1	1	1	$\frac{V_{dc}}{2}$
2	0	0	0	0	0	1	0	1	1	1	1	1	$\frac{V_{dc}}{3}$
3	0	0	0	0	1	1	0	0	1	1	1	1	$\frac{V_{dc}}{6}$
4	0	0	0	1	1	1	0	0	0	1	1	1	0
5	0	0	1	1	1	1	0	0	0	0	1	1	$-\frac{V_{dc}}{6}$
6	0	1	1	1	1	1	0	0	0	0	0	1	$-\frac{V_{dc}}{3}$
7	1	1	1	1	1	1	0	0	0	0	0	0	$-\frac{V_{dc}}{2}$

Submodule Capacitor Voltage Balancing

The SM's capacitor voltage should be regulated at V_{dc}/m, where m denotes the SM's number in an arm and V_{dc} represents input DC voltage. The PWM cannot ensure the voltage balance of the capacitors because it does not take into account the voltage of the submodule capacitors. Therefore, to regulate the SMs capacitor voltage, the gating pattern must be modified dependent on the voltage level, arm current, and voltage of the SMs capacitor. The capacitor voltage balancing algorithm has four stages: i. Capacitor voltage's sorting ii. Determining the direction of arm currents iii. Selecting suitable submodules iv. Generating gate pulses.

Capacitor voltage sorting entails measuring submodule capacitor voltages in an MMC leg and arranging them in descending order. The arm current's direction flowing through the submodule affects the charging characteristics of capacitors. In the insertion mode, when the submodule is ON and the arm current is positive, the capacitor gets charged. When the submodule is OFF, the capacitor discharges for the negative arm current. In the bypassed mode, when the submodule is OFF, the capacitor voltage keeps unchanged regardless of the arm current direction. The stage of submodule selection involves choosing the number of submodules from the upper and lower arms based on switching states of MMC.

IV. RESULTS AND DISCUSSION

To verify the UCMS-PD PWM effectiveness, simulation models of 7-level and 5-level MMC along with capacitor voltage balance algorithm are designed in MATLAB Simulink platform respectively. The simulation parameters of MMC are listed in **Table 2.** The remaining parameters including reference and carrier signals of PD, POD and APOD PWM are listed in **Table 3**. And the carrier frequency (switching frequency) is set as 3000 Hz.

Table 2. Simulation Parameters of MMC

S. No	Parameters	Symbol	Value	Unit
1	Power rating	P_r	0.5	KVA
2	DC Voltage	V_{dc}	660	V
3	SM Capacitance	C_{sm}	100	μF
4	Arm Resistance	R_{arm}	0.1	Ω
5	Arm Inductance	L_{arm}	3.8	mH
6	Total No of SMs	m	6	-
7	Load	*R-L*	105.8 and 2.5	Ω ,mH

Table 3. Simulation Parameters of PD, POD and APOD PWM

Sl. No	Parameters	Value	Unit
1	Reference sinusoidal waveform amplitude	[3/3, 0, -3/3]	V
2	Carrier triangular waveform amplitude for UCMS- PD PWM	C_1-[2/3, 3/3, 2/3],C_2-[1/3, 2/3, 1/3],C_3-[0, 1/3, 0], C_4-[-1/3, 0, -1/3],C_5-[-2/3, -1/3, -2/3],C_6-[-3/3, -2/3, -3/3]	V
3	Carrier triangular waveform amplitude for POD PWM	C_1-[2/3,3/3 ,2/3],C_2-[1/3, 2/3,1/3],C_3-[0,1/3, 0], C_4-[0, -1/3, 0],C_5-[-1/3, -2/3,-1/3],C_6-[-2/3, -3/3, -2/3]	V
4	Carrier triangular waveform amplitude for APOD PWM	C_1-[2/3, 3/3,2/3],C_2-[2/3, 1/3, 2/3],C_3-[0, 1/3, 0], C_4-[0 ,-1/3,0],C_5-[-2/3, -1/3, -2/3],C_6-[-2/3, -3/3, -2/3]	V
5	Reference frequency	50	Hz
6	Carrier frequency	3000	Hz

The different level shift PWM techniques are implemented on MMC, and the output voltage quality is analyzed using % THD for various modulation indices. **Table 4** shows the fundamental voltage magnitude in Volts (V) and Total harmonic distortion in percentage (THD) results on 1-phase 7-level MMC for POD, APOD and UCMS-UCMS-PD PWM control method. The triangle carrier frequency of these PWM techniques is 3000Hz, and Amplitude modulating indices vary from zero to one. The UCMS- PD PWM gives better fundamental voltage magnitude and Voltage THD rather than POD and APOD PWM for seven levels (6 SM per arm). The reason is that the overlapping period between the PD pulses is greater than the pulses of POD and APOD. Consequently, UCMS-PD PWM provides more power to common-mode voltage of MMC. The output phase voltage (V_{o_ph}) of a symmetrical load in the MMC is the difference between leg voltage (V_{leg}) and common-mode voltage (V_{cmv}) in MMC. The leg voltage power is the same for PD, POD and APOD PWM. Hence phase voltage power produced by the UCMS-PD PWM contains less power distortion rather than those produced by the POD and APOD PWM. In the lower values of modulation indices (m_a= 0.1 to 0.5), the % THD increases, and fundamental voltage decreases at a higher rate.

Table 4 . Harmonic analysis of 1-Φ MMC (SMs = 6 per arm)

SMs per arm = 6 , Reference frequency, f_r = 50 Hz						
Modulating indices (M_a)	**PD- PWM**		**POD- PWM**		**APOD- PWM**	
	THD (%)	**V_{fu}**	**THD(%)**	**V_{fu}**	**THD(%)**	**V_{fu}**
0.1	110.55	32.25	115.23	31.6	111.69	31.48
0.2	64.35	65	68.88	66.38	65.05	66.39
0.3	36.44	97.6	41.45	95.23	37.78	94.86
0.4	23.02	130	30.34	128.4	25.38	132.1
0.5	18.88	164.1	26.38	161.8	21.68	166.5
0.6	14.86	197.1	21.46	196.1	16.7	196.5
0.7	10.09	227.9	15.66	225.3	11.75	225.8
0.8	8.42	263.6	14.52	260.9	10.13	259.9
0.85	7.41	280	13.27	280.2	9.36	279.8
0.9	6.7	294.6	12.38	290	8.74	291
0.95	5.28	316.1	10.45	312	6.66	313.5
1	4.41	328.64	9.2	324.87	5.25	326.24

Fig 4. Comparison Chart of %THD Versus Modulation Indices for Modified LS PWM Techniques**.**

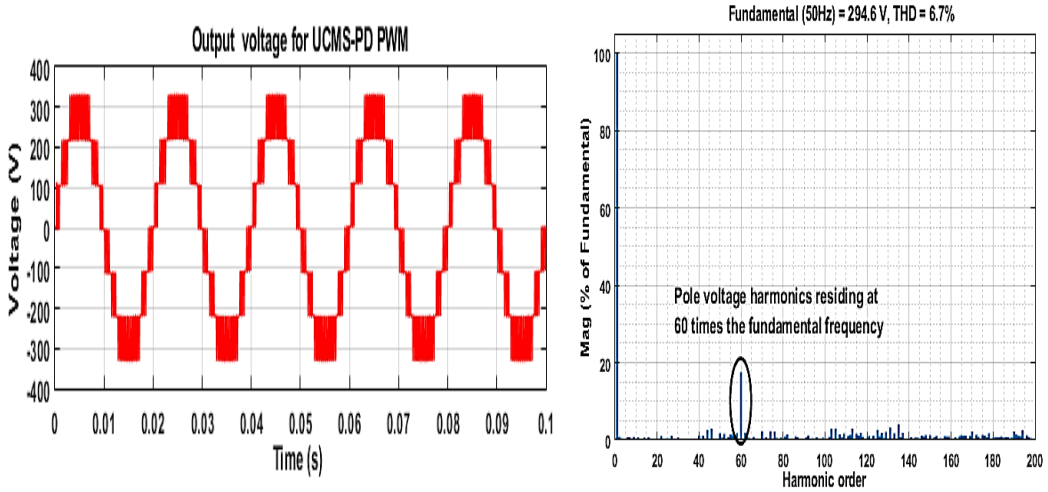


Fig 5. Output Phase Voltage and Harmonic Profile For UCMS-UCMS-PD PWM
(6 submodules per arm, m_a = 0.9, f_c= 3000Hz)

The simulation results of load phase voltage waveform and voltage THD (%) simulation waveform for PD for m_a = 0.9 and m_f= 60 are shown in **Fig 5**. From the %THD spectrum of PD PWM, the first band of pole voltage harmonics residing at harmonic order 60, which frequency is 3000Hz (60 times the fundamental frequency).The following section describes the effects of combined submodule switching pulses of UCMS based PD ,APOD and POD PWM techniques.These switching pulses are illustrated in **Fig 6**. It is inferred that the each submodule's switching pattern is not the same. Consequently, loss distribution is not the same for submodules. Hence balancing of submodule capacitor voltage is required.

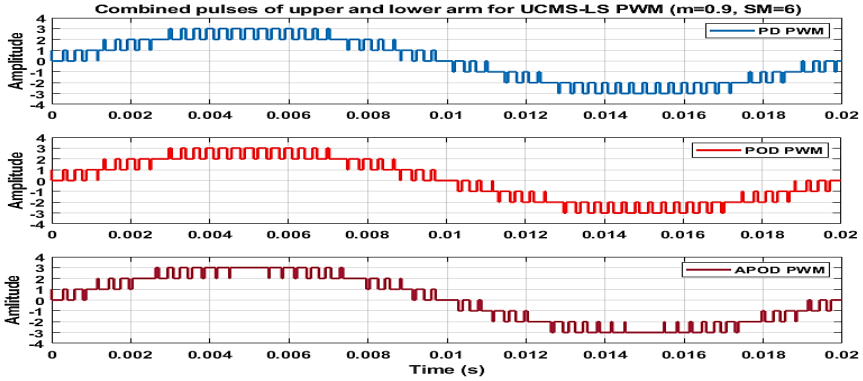
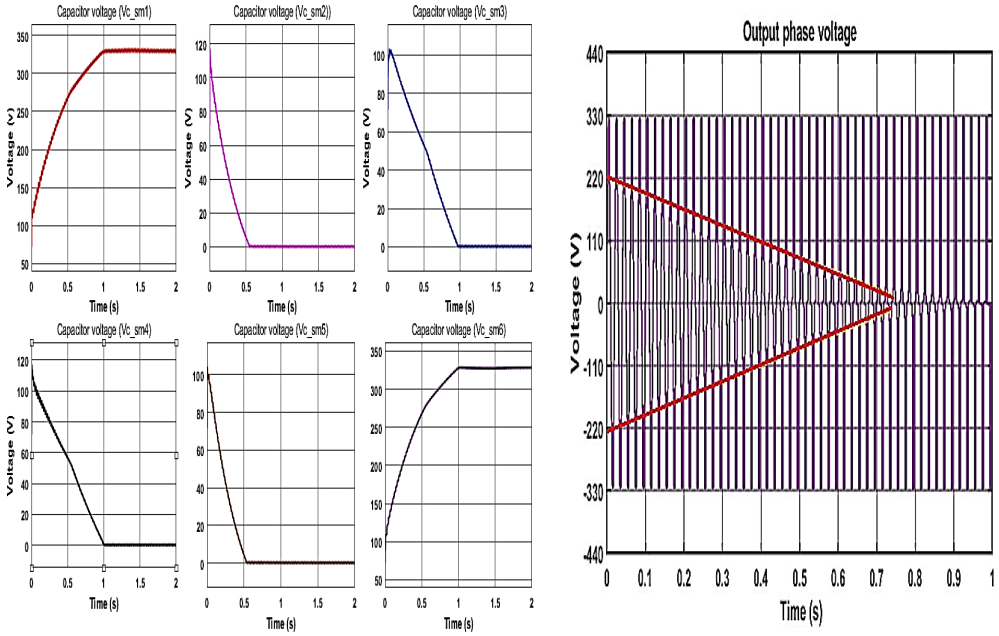


Fig 6. Combined Pulses For PD, POD and APOD PWM.

This section explores the simulation analysis of capacitor voltage regulating in MMC. The sorting based algorithm is employed to balance the SM's capacitor voltage. The voltage across the capacitor during the operation should be $\frac{V_{dc}}{n-1}$ i.e., 110V. **Fig 7 (a)** and **(b**) depict the divergence of capacitors voltage when MMC is not applied to any sorting algorithm. In **Fig 7(a),** the capacitor voltages of V_{c_sm1} and V_{c_sm6} increase to 330 V at 1 second. On the other hand, the capacitor voltages of V_{c_sm2},V_{c_sm3}, V_{c_sm4} and V_{c_sm5} reduce to 0 V at 1 second. The effect of divergence of capacitor voltages is reflected in phase voltage in the output. It is illustrated in **Fig 7 (b).** The phase voltage maintains its seven levels up to 0.05 seconds. Then the output level reduces and ends at two levels.



(a) (b)

Fig 7. (a). Upper Arm Submodule Capacitor Voltages on MMC With Absence of Capacitor Voltage Control, (b). Output Phase Voltage On MMC With Absence Capacitor Voltage Control.

The simulation results for seven-level MMC with capacitor voltage balancing using a sorting algorithm are shown in **Fig 8** and **9**. These figures illustrate the capacitor voltages of submodules (V_{c_sm1}, V_{c_sm2}, V_{c_sm3}, V_{c_sm4}, V_{c_sm5} and V_{c_sm6}). Voltages of the capacitors are regulated at 110 V. Consequently, the seven output levels are maintained during the operation period. However, ripples are present in the capacitor voltages due to the circulation current in the MMC's phase leg. The capacitor voltage oscillates between 122 V and 102 V. The SM's capacitor voltage is regulated at 110 V with 16 V_{pp} voltage ripples (14.5%). The summation voltages of lower arm and upper arm are illustrated in **Fig 10**. The capacitor average voltage is 660 V, i.e., input DC voltage.

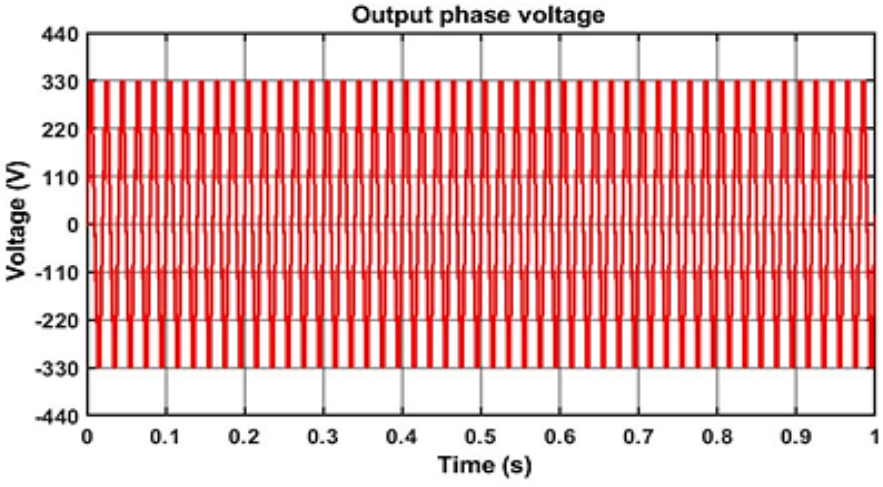


Fig 8. Output Phase Voltage on MMC With Capacitor Voltage Balancing.

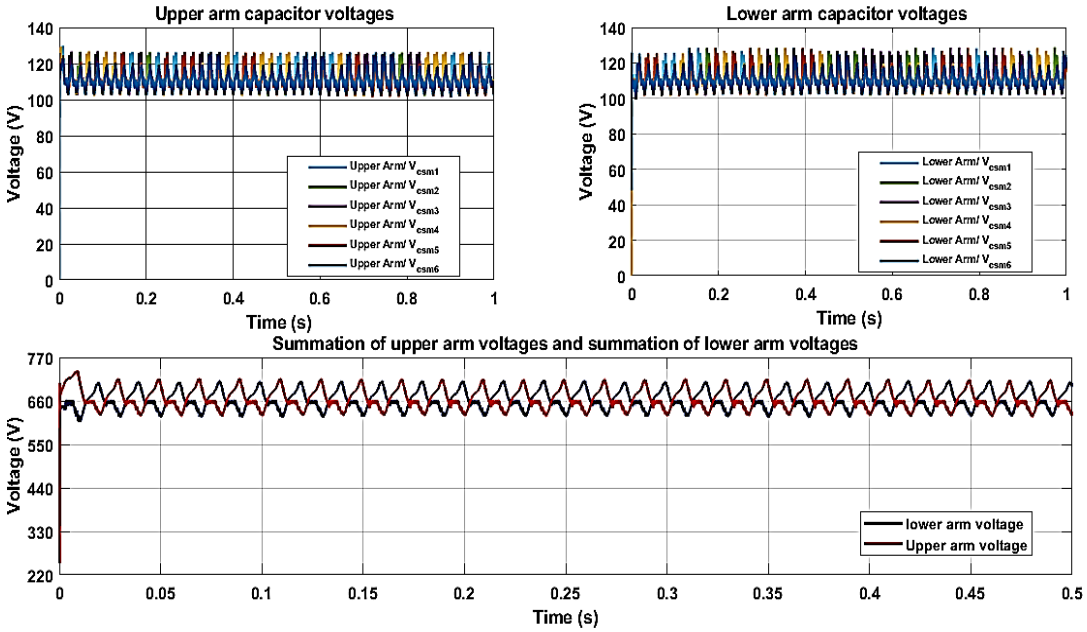


Fig 9. Upper Arm Submodule Capacitor Voltages on MMC with Capacitor Voltage Control.

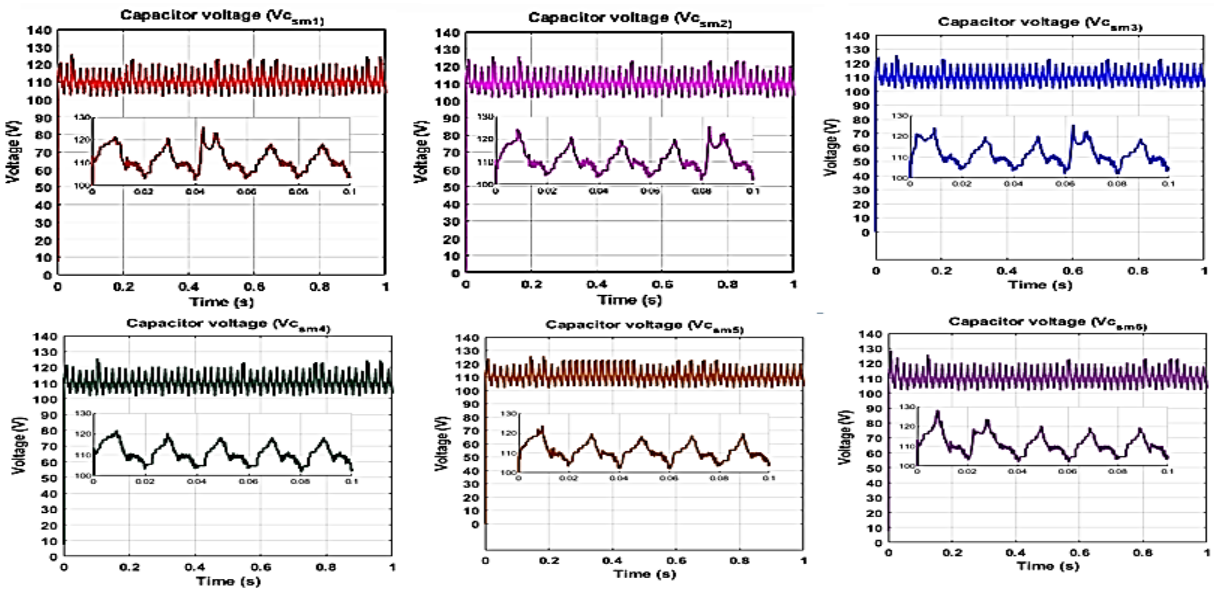


Fig 10. MMC's Arm Capacitor Voltages.

V. EXPERIMENTAL VALIDATION

The 1-Φ seven-level MMC is implemented by a prototypical laboratory setup for the power rating of 500 Watts and the control algorithms of level-shift PWM and capacitor voltage balancing are developed in the MATLAB / Simulink platform. **Fig 11** illustrates the prototype hardware view of 1-Φ seven-level MMC. The main ideology behind the experimental hardware implementation is Hardware-In-Loop (HIL) based control of the MMC. The switching device's pulses are generated using the dSPACE - DS1202 with the Control Desk platform as the front end and MATLAB / RTI as the backend. Also, the voltage and current signals sensed from the various sensors are connected to the MicroLabBox connector panel and will be given to the Control Desk for processing and running the developed algorithm.

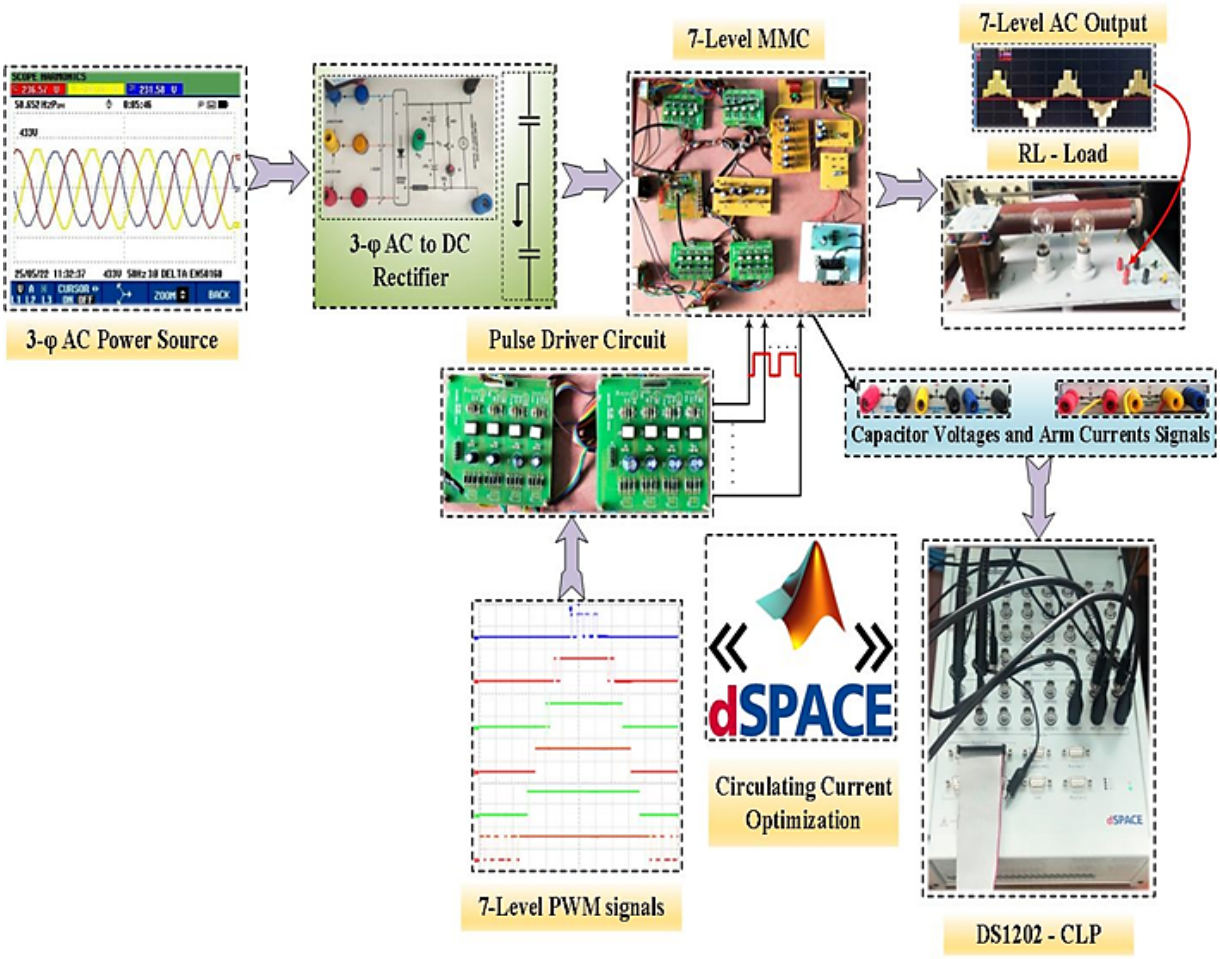


Fig 11. Block Diagram of The Hardware Structure.

Table 5. Hardware Parameters

Output Voltage (V_{out})	**230 V**
DC Bus Voltage (V_{dc})	660 V
Number of SMs per Arm (N)	6
SM Capacitance (C_{sm})	100 μF
SM's Capacitor Voltage (V_c)	165 V
Arm Inductance (L_{arm})	3.5 mH , 5 Ampere
Carrier frequency (f_c)	3000 Hz
Reference Signal Frequency (f_r)	50 Hz
Load ($R-L$)	R= 105.8 Ω , L= 2.5 mH, 5 Ampere
MOSFET (IRF840)	500V/8A, Switching frequency 1 MHz
pulse driver circuit board (TLP250)	Gate-source voltage 15VGS to 20VGS, frequency 25 kHz.

The hardware results of harmonic profile for POD, APOD and UCMS-PD PWM schemes are depicted in the **Fig 12**. Total harmonic distortion for the UCMS-PD PWM in the single phase MMC is lesser than POD and APOD. The table compares simulation and hardware results for the LS-PWM techniques POD, APOD, and PD. The UCMS-PD PWM exhibits a superior harmonic profile compared to POD and APOD PWM. The total harmonic distortion of the load phase voltage and load phase current is lower with UCMS-PD PWM than with POD and APOD PWM. **Table 5.** shows Hardware Parameters.

Table 6. Comparative harmonics analysis of PD, POD and APOD PWM techniques in 1-Φ MMC (Fundamental frequency = 50Hz)

PWM	Harmonics			
	Simulation		**Hardware**	
	THD %	**V_{rms}**	**THD %**	**V_{rms}**
PD	**6.57**	**229.7**	**7.0**	**226**
POD	**12.38**	**225.6**	**14.5**	**221**
APOD	**8.74**	**227.4**	**10.9**	**224**

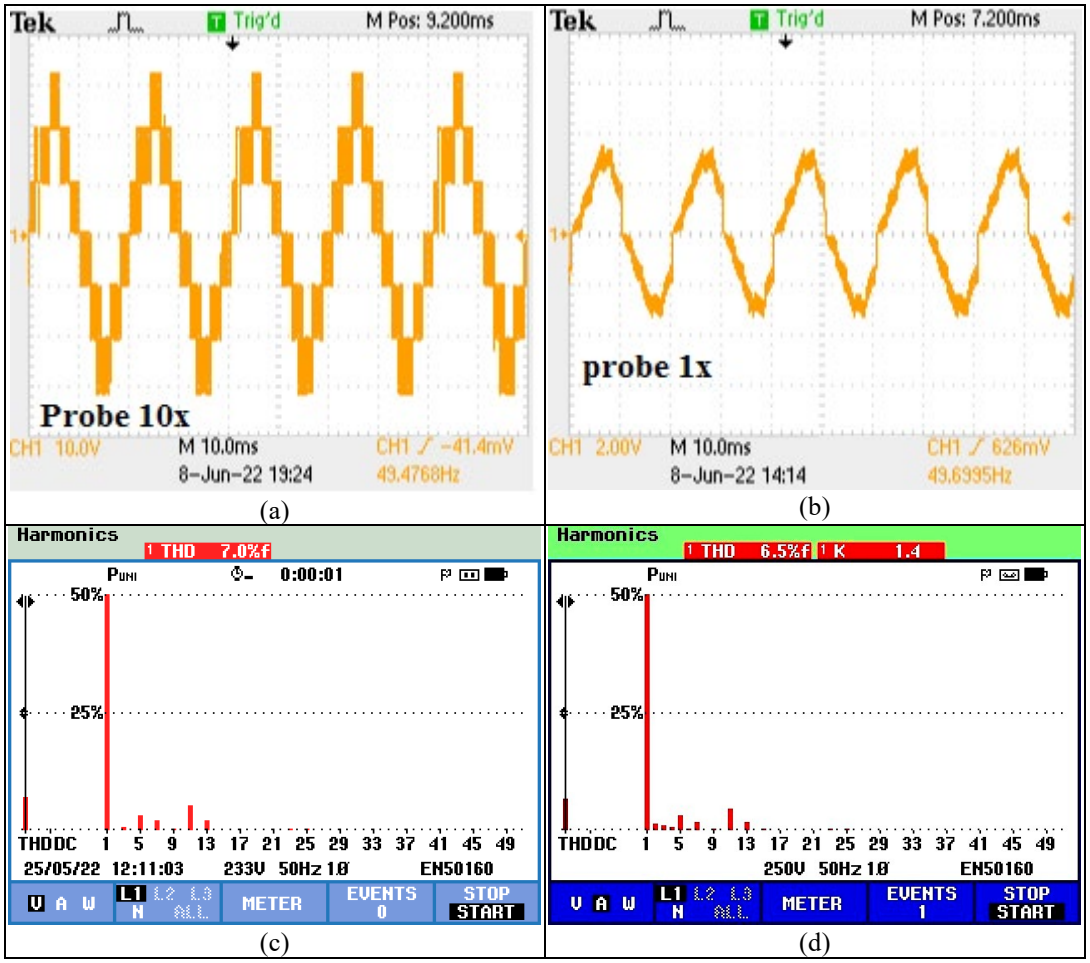


Fig 12. Hardware Outcomes Using UCMS-PD PWM for 1-Φ seven-level MMC (m_a=0.9) (i) Load Voltage (v_{o_ph}) (ii) Load Current (i_{o_ph}) (iii) % THD of v_{o_ph} (iv) %THD of i_{o_ph}.

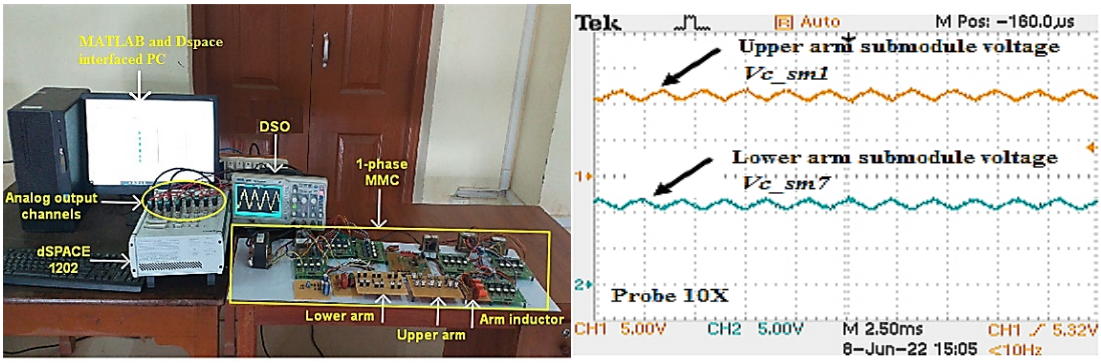


Fig 13. (a) Hardware Image Of the Proposed System (b) Hardware Results of Capacitor Voltages For UCMS- PD PWM fed 1-Φ Seven Level MMC.

Capacitor voltage control using sorting algorithm is applied along with the UCMS- PD PWM to the proposed 1-Φ seven level MMC. The value of submodule capacitor voltages should be balanced at 110 V. This voltage value is calculated as $\frac{V_{dc}}{n-1}$ V, where V_{dc} denotes input dc voltage (660 V), and n represents number of level. It is illustrated in the **Fig 13(b).** The green and red coloured waveforms in the **Fig 13(b)** depict the upper and the lower arm submodule capacitor voltages, respectively. These capacitor voltages oscillate between 100 V to 120 V. The causes for the oscillation are due to the circulating current flowing in the MMC's leg. **Table 6.** Shows Comparative harmonics analysis of PD, POD and APOD PWM techniques in 1-Φ MMC (Fundamental frequency = 50Hz)

VI. CONCLUSION

This work applies a Universal Control Modulation Scheme (UCMS)-based modified level shift PWM technique and a sorting algorithm-based capacitor voltage control method to a seven-level 1-Φ MMC to analyze its performance. The MMC prefers this PWM technique due to its ability to manage multiple switches efficiently and effortlessly, which is made possible by the presence of multiple carriers. The performance outcomes are assessed and compared with those of three distinct PWM techniques: phase disposition, phase opposition disposition, and alternate phase opposition disposition. Simulation models of 1-Φ MMC for six submodules per arm are developed in MATLAB/Simulink. The output voltage's quality is analysed using the performance of total harmonic distortion (% THD) with various modulation indices. In level shift PWM techniques, the first band of harmonics is moved to the frequency that is the product of the fundamental frequency and the frequency modulation index. The phase disposition PWM provides a better harmonic profile (V_f =294.6 V and THD = 6.7%) of output phase voltage than the phase opposition disposition(V_f =290V and THD = 12.38%) and alternate phase opposition disposition(V_f =291 V and THD = 8.74%). Next, a sorting algorithm implements the submodule's capacitor voltage control in conjunction with UCMS-PD PWM. Effectively, this algorithm regulates the capacitors' voltages at 110 V. Finally, the simulation results are validated using an experimental prototype of MMC with the hardware-in-loop-based dSPACE MicroLabBox 1202. This solidifies the effectiveness of the suggested PWM techniques and capacitor voltage balancing algorithm.

Data Availability

No data was used to support this study.

Conflicts of Interests

The author(s) declare(s) that they have no conflicts of interest.

Funding

No funding agency is associated with this research.

Competing Interests

There are no competing interests.

References

[1]. S. Haq, S. P. Biswas, Md. K. Hosain, Md. A. Rahman, Md. R. Islam, and S. Jahan, "A Modular Multilevel Converter with an Advanced PWM Control Technique for Grid-Tied Photovoltaic System," Energies, vol. 14, no. 2, p. 331, Jan. 2021, doi: 10.3390/en14020331.

[2]. C. Burgos-Mellado et al., "Cyber-Attacks in Modular Multilevel Converters," IEEE Transactions on Power Electronics, vol. 37, no. 7, pp. 8488–8501, Jul. 2022, doi: 10.1109/tpel.2022.3147466.

[3]. Y. Hou and Y. Wang, "Optimization of Capacitor Voltage Control Strategy for MMC Sub-module," Journal of Physics: Conference Series, vol. 2166, no. 1, p. 012036, Jan. 2022, doi: 10.1088/1742-6596/2166/1/012036.

[4]. S. Kamal et al., "Particle Swarm Optimization and Modular Multilevel Converter Communication in Electrical Applications with Machine Learning Algorithm," Computational Intelligence and Neuroscience, vol. 2022, pp. 1–11, Jun. 2022, doi: 10.1155/2022/8516928.

[5]. E. Barbie, R. Rabinovici, and A. Kuperman, "Analytical formulation and optimization of Weighted Total Harmonic Distortion in three-phase staircase modulated multilevel inverters," Energy, vol. 215, p. 119137, Jan. 2021, doi: 10.1016/j.energy.2020.119137.

[6]. M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, and R. P. Aguilera, "Modular Multilevel Converters: Recent Achievements and Challenges," IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 224–239, 2021, doi: 10.1109/ojies.2021.3060791.

[7]. Y. Xin, C. Chen, L. Sun, L. Zhou, J. Xiong, and K. Zhang, "Module selection method with improved capacitor voltage balance for MMC using (2 N + 1) SHEPWM," International Journal of Electrical Power & Energy Systems, vol. 133, p. 107294, Dec. 2021, doi: 10.1016/j.ijepes.2021.107294.

[8]. L. A. M. Barros, M. Tanta, A. P. Martins, J. L. Afonso, and J. G. Pinto, "Submodule Topologies and PWM Techniques Applied in Modular Multilevel Converters: Review and Analysis," Sustainable Energy for Smart Cities, pp. 111–131, 2021, doi: 10.1007/978-3-030-73585-2_8.

[9]. A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A Space-Vector PWM-Based Voltage-Balancing Approach With Reduced Current Sensors for Modular Multilevel Converter," IEEE Transactions on Industrial Electronics, vol. 63, no. 5, pp. 2734–2745, May 2016, doi: 10.1109/tie.2016.2514346.

[10]. S. Du, J. Liu, and T. Liu, "Modulation and closed-loop-based dc capacitor voltage control for mmc with fundamental switching frequency," IEEE Trans. Power Electron., vol. 30, no. 1, pp. 327–338, Jan 2015

[11]. S. Du, A. Dekka, B. Wu, and N. Zargari, Modular Multilevel Converters: Analysis, Control, and Applications. John Wiley & Sons, Inc., 2017. doi: 10.1002/9781119367291.

[12]. E. Solas, G. Abad, J. A. Barrena, A. Carear, and S. Aurtenetxea, "Modelling, simulation and control of Modular Multilevel Converter," Proceedings of 14th International Power Electronics and Motion Control Conference EPE-PEMC 2010, Sep. 2010, doi: 10.1109/epepemc.2010.5606881.

[13]. A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 4, pp. 1631–1656, Dec. 2017, doi: 10.1109/jestpe.2017.2742938.

[14]. S. Debnath, J. Qin, and M. Saeedifard, "Control and Stability Analysis of Modular Multilevel Converter Under Low-Frequency Operation," IEEE Transactions on Industrial Electronics, vol. 62, no. 9, pp. 5329–5339, Sep. 2015, doi: 10.1109/tie.2015.2414908.

[15]. R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "Controllers for eliminating the ac components in the circulating current of modular multilevel converters," IET Power Electronics, vol. 9, no. 1, pp. 1–8, Jan. 2016, doi: 10.1049/iet-pel.2014.0930.

[16]. Y. Okazaki, H. Matsui, M. Hagiwara, and H. Akagi, "Design considerations on the DC capacitor of each chopper cell in a modular multilevel cascade inverters (MMCI-DSCC) for medium-voltage motor drives," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2014, doi: 10.1109/ecce.2014.6953861.

[17]. M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," IEEE Transactions on Power Electronics, vol. 24, no. 7, pp. 1737–1746, Jul. 2009, doi: 10.1109/tpel.2009.2014236.

[18]. D. Ronanki and S. S. Williamson, "Failure Prediction of Submodule Capacitors in Modular Multilevel Converter by Monitoring the Intrinsic Capacitor Voltage Fluctuations," IEEE Transactions on Industrial Electronics, vol. 67, no. 4, pp. 2585–2594, Apr. 2020, doi: 10.1109/tie.2019.2912771.

[19]. Z. A. Aljawary, S. de Pablo, L. C. Herrero-de Lucas, and F. Martinez-Rodrigo, "Local Carrier PWM for Modular Multilevel Converters with Distributed PV Cells and Circulating Current Reduction," Energies, vol. 13, no. 21, p. 5585, Oct. 2020, doi: 10.3390/en13215585.

[20]. Y. Zhang, K. Dai, C. Xu, Y. Kang, and Z. Dai, "Multiple sampling PSC-PWM with hierarchical control architecture for MMC-DSTATCOM," IET Electric Power Applications, vol. 13, no. 10, pp. 1431–1440, Jun. 2019, doi: 10.1049/iet-epa.2018.5784.

[21]. H. B. Gobburi, V. B. Borghate, and P. M. Meshram, "Discontinuous Pulse Width Modulation Techniques for Modular Multilevel Converter," 2020 IEEE International Students' Conference on Electrical,Electronics and Computer Science (SCEECS), Feb. 2020, doi: 10.1109/sceecs48394.2020.57.

[22]. M. Kurtoğlu, F. Eroğlu, A. O. Arslan, and A. M. Vural, "Recent contributions and future prospects of the modular multilevel converters: A comprehensive review," International Transactions on Electrical Energy Systems, vol. 29, no. 3, p. e2763, Nov. 2018, doi: 10.1002/etep.2763.

[23]. G. Konstantinou, J. Pou, S. Ceballos, R. Darus, and V. G. Agelidis, "Switching Frequency Analysis of Staircase-Modulated Modular Multilevel Converters and Equivalent PWM Techniques," IEEE Transactions on Power Delivery, vol. 31, no. 1, pp. 28–36, Feb. 2016, doi: 10.1109/tpwrd.2015.2416759.

[24]. V. L. Narla, R. Kachhoria, M. Arun, A. H, D. Vijendra Babu, and B. M. Jos, "IoT based energy efficient multipath power control for underwater sensor network," International Journal of System Assurance Engineering and Management, Apr. 2022, doi: 10.1007/s13198-021-01560-7.

[25]. D. De Simone, P. Tricoli, S. D'Arco, and L. Piegari, "Windowed PWM: A Configurable Modulation Scheme for Modular Multilevel Converter-Based Traction Drives," IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9727–9736, Sep. 2020, doi: 10.1109/tpel.2020.2969375.